



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,989	10/17/2000	Yoshitaka TSUNASHIMA	04329.1952-01000	2408
22852	7590	07/21/2005	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413				RAO, SHRINIVAS H
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/688,989	TSUNASHIMA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 27 May 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 27,28 and 30-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 27,28 and 30-33 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

Applicants' request for RCE filed on April 14, 2005 along with an amendment and the supplemental amendment filed on May 18, 2005 have been entered and forwarded to the Examiner on May 27, 2005.

Therefore claim 28 as amended by the supplemental amendment filed on May 18, 2005 and claim 27, 30-33 as originally filed are currently pending in the Application. Claims 1-26 and 29 has been cancelled by amendments.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 27 –28 and 30-33 are rejected under 35 U.S.C. 102(b) as being anticipated by De La Moneda et al. ( U.S. Patent No. 4,445,267, herein after De La Moneda).

With respect to claim 27 De La Moneda describes a semiconductor device comprising: a semiconductor substrate including a first and second region separated by an isolation element; ( De La Moneda figs. 1-1 # 10-substrate , figs. #12 isolation element col. 4 lines 20-25 etc.) a first transistor formed on the first region of the substrate ( claim 7 , col. 6 lines 35-40) and including a first insulation film ( figs. # 16 , col. 4 lines 27-28) and a first gate electrode arranged along a first direction, ( figures (

Art Unit: 2814

figs. 3 20 etc.) and a second transistor formed on the second region of the substrate and including a second insulation film and a second gate electrode arranged along the first direction, ( figs. Structure above 18) wherein a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction. ( fig 10 # 42 connecting over isolation element 12).

With respect to claim 28, De La Moneda describes a device according to claim 33, wherein a side of the side insulator film is on a surface of said semiconductor . ( De La Moneda figures e.g. fig. 10 #38 , col. 12-16) .

With respect to claim 30 De La Moneda describes a device according to claim 28, wherein at least one of said first and second gate electrodes is formed by a damascene gate process. (De La Moneda figures 1-11 , same as Applicants' description at least at page 9 lines 10-25 and page 26 lines 2 to 20 for their gate formation) .

With respect to claim 31 De La Moneda describes a device according to claim 33, wherein said first insulation film is thinner than said second insulation film, said first transistor forms a logic circuit, and said second transistor forms a memory cell. ( De La Moneda figures, col.2 lines 30-36).

With respect to claim 32 De La Moneda describes a device according to claim 33, wherein top surfaces of said first and second gate electrodes are coplanar. ( De La Moneda figures).

With respect to claim 33 De La Moneda describes a device according to claim 27, wherein said second transistor further comprises a polysilicon layer formed on the second insulation film formed on the substrate, (De La Moneda figure 10 # 20 over 16) and a side insulator film formed on a side of the second insulation film and a side wall of the polysilicon layer, (De La Moneda figure 10 # 38 ) said second gate electrode is formed on the polysilicon layer, (De La Moneda figure 10 ) the side wall of said first gate electrode is directly connected to a side wall of said second gate electrode ( De La Moneda figure 10) and connected to the side wall of the second insulation film and the side wall of the polysilicon layer via the side insulator film substrate. ( De La Moneda figures specifically 10 and col. 6-7 ).

***Response to Arguments***

Applicant's arguments with respect to claims 27-28,30-33 have been considered but are moot in view of the new ground(s) of rejection.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.00 to 5.00.

Art Unit: 2814

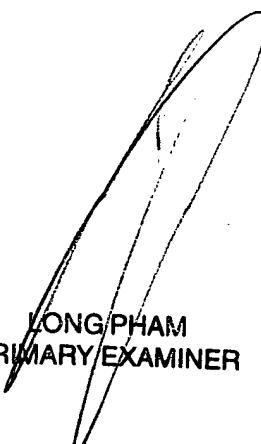
The fax phone number for the organization where this application or proceeding  
is assigned is 703-872-9306.



Steven H. Rao

Patent Examiner

July 13, 2005.



LONG PHAM  
PRIMARY EXAMINER